IN THE CLAIMS

Please cancel claims 14 and 30.

Please amend claims 1, 9, 15, 20, 22, and 29 as follows:

1. (Currently Amended) A clock stop detector for a memory for detecting a clock signal being not active for a predetermined period of time, the clock stop detector comprising:

a first switch that closes in response to a first logic level of ~~a~~an inverted clock signal to charge a capacitor;

a second switch that closes in response to a second logic level of the inverted clock signal to discharge the capacitor; and

a logic circuit that receives the clock signal and a charge signal based on a charge on the capacitor, and that outputs a control signal indicating when the clock signal was not active for a period of time exceeding the predetermined period of time, ~~based on an inverted clock signal and a charge signal based on a charge on the capacitor,~~

~~wherein the capacitor is selected such~~

~~that the capacitor is not discharged to a point where the charge signal transitions, when the inverted clock signal is active, and~~

~~that the capacitor is discharged to the point where the charge signal transitions, when the inverted clock signal is not active.~~

wherein the capacitor is charged to the second logic level when the inverted clock signal is at the first logic level, and

wherein the capacitor is discharged to the first logic level when the inverted clock signal is at the second logic level for a period of time exceeding the predetermined period of time.

2. (Original) The clock stop detector of claim 1, wherein the first switch comprises a first transistor and the second switch comprises a second transistor.

3. (Original) The clock stop detector of claim 2, wherein the first transistor is a p-type metal-oxide semiconductor field effect transistor and the second transistor is an n-type metal-oxide semiconductor field effect transistor.

4. (Original) The clock stop detector of claim 1, wherein the logic circuit comprises a NOR gate.

5. (Original) The clock stop detector of claim 1, wherein the first logic level is a logic low logic level and the second logic level is a logic high logic level.

6. (Original) The clock stop detector of claim 1, further comprising:

a current source coupled to the second switch to discharge the capacitor if the second switch is closed.

7. (Original) The clock stop detector of claim 1, further comprising:

a power supply voltage coupled to the first switch to charge the capacitor if the first switch is closed.

8. (Original) The clock stop detector of claim 1, wherein the second switch is open if the first switch is closed and the first switch is open if the second switch is closed.

9. (Currently Amended) A memory comprising:

a clock stop detector for detecting a clock signal being not active for a predetermined period of time, the clock stop detector configured to receive athe clock signal and output a control signal in response to the clock signal; and

a peripheral circuit for reading and writing data to a memory bank, wherein the peripheral circuit is configured to receive the control signal and activate and deactivate in response to the control signal,

~~wherein the clock stop detector comprises a capacitor and outputs the control signal based on the clock signal and a charge signal based on the charge on the capacitor, and~~

~~wherein the capacitor is selected such~~

~~that the capacitor is not discharged to a point where the charge signal transitions, when the clock signal is active, and~~

~~that the capacitor is discharged to the point where the charge signal transitions, when the clock signal is not active.~~

wherein the clock stop detector comprises:

a first switch that closes in response to a first logic level of an inverted clock signal to charge a capacitor;

a second switch that closes in response to a second logic level of the inverted clock signal to discharge the capacitor; and

a logic circuit that receives the clock signal and a charge signal based on a charge on the capacitor, and that outputs a control signal indicating when the clock signal was not active for a period of time exceeding the predetermined period of time,

wherein the capacitor is charged to the second logic level when the inverted clock signal is at the first logic level, and

wherein the capacitor is discharged to the first logic level when the inverted clock signal is at the second logic level for a period of time exceeding the predetermined period of time.

10. (Original) The memory of claim 9, further comprising:

a clock receiver configured to receive an external clock signal and pass the clock signal to the clock stop detector.

11. (Original) The memory of claim 9, further comprising:

an address receiver configured to receive the control signal and activate and deactivate in response to the control signal.

12. (Original) The memory of claim 9, further comprising:

a command receiver configured to receive the control signal and activate and deactivate in response to the control signal.

13. (Original) The memory of claim 9, a data receiver and driver configured to receive the control signal and activate and deactivate in response to the control signal.

14. (Cancelled)

15. (Currently Amended) The memory of claim ~~14~~9, wherein the first switch comprises a first transistor and the second switch comprises a second transistor.

16. (Original) The memory of claim 9, wherein the memory comprises a random access memory.

17. (Original) The memory of claim 9, wherein the memory comprises a dynamic random access memory.

18. (Original) The memory of claim 9, wherein the memory comprises a double data rate synchronous dynamic random access memory.

19. (Original) The memory of claim 9, wherein the memory comprises a mobile random access memory.

20. (Currently Amended) A clock stop detector for a memory for detecting a clock signal being not active for a predetermined period of time, the clock stop detector comprising:

means for receiving a clock signal and an inverted clock signal;

means for charging a capacitor in response to a first logic level of the inverted clock signal;

means for discharging the capacitor in response to a second logic level of the inverted clock signal; and

means for providing a control signal indicating when the clock signal was not active for a period of time exceeding the predetermined period of time based on the clock signal and a charge signal based on a charge on the capacitor, the means for providing the control signal receiving the clock signal and the charge signal, and

~~wherein the capacitor is selected such~~

~~that the capacitor is not discharged to a point where the charge signal transitions, when the clock signal is active, and~~

~~that the capacitor is discharged to the point where the charge signal transitions, when the clock signal is not active.~~

wherein the capacitor is charged to the second logic level when the inverted clock signal is at the first logic level, and

wherein the capacitor is discharged to the first logic level when the inverted clock signal is at the second logic level for a period of time exceeding the predetermined period of time.

21. (Original) The clock stop detector of claim 20, further comprising:

means for providing the control signal to memory circuits to deactivate and activate the memory circuits in response to the control signal.

22. (Currently Amended) A method for detecting a stopped clock signal in a memory comprising:

receiving a clock signal and an inverted clock signal;

charging a capacitor in response to a first logic level of the inverted clock signal;

discharging the capacitor in response to a second logic level of the inverted clock signal; and

detecting a stopped clock signal based on the clock signal and a charge signal based on a charge on the capacitor,

wherein the step of detecting the stopped clock signal comprises receiving the clock signal and the charge signal and detecting the stopped clock signal based on the received clock signal and the charge signal,

~~wherein the capacitor is selected such~~

~~that the capacitor is not discharged to a point where the charge signal transitions, when the clock signal is active, and~~

~~that the capacitor is discharged to the point where the charge signal transitions, when the clock signal is not active.~~

wherein the capacitor is charged to the second logic level when the inverted clock signal is at the first logic level, and

wherein the capacitor is discharged to the first logic level when the inverted clock signal is at the second logic level for a period of time exceeding a predetermined period of time.

23. (Original) The method of claim 22, wherein charging the capacitor comprises closing a first switch to supply a voltage to the capacitor.

24. (Original) The method of claim 23, wherein the first switch comprises a transistor.

25. (Original) The method of claim 22, wherein discharging the capacitor comprises closing a second switch to sink a current from the capacitor.

26. (Original) The method of claim 25, wherein the second switch comprises a transistor.

27. (Original) The method of claim 25, further comprising:
providing a control signal in response to detecting the stopped clock signal.

28. (Original) The method of claim 27, further comprising:

deactivating a memory circuit in response to the control signal.

29. (Currently Amended) A portable electronic device comprising:

a controller configured to output a clock signal that starts and stops in response to user commands to a portable electronic device; and

a memory that receives the clock signal, the memory comprising:

a clock stop detector configured to output a clock stop signal in response to the clock signal being not active for a predetermined period of time;

a peripheral circuit configured to receive the clock stop signal and activate and deactivate in response to the clock stop signal; and

a memory bank configured to receive address signals, control signals, and data signals from the peripheral circuit for reading and writing data in the memory bank,

~~wherein the clock stop detector comprises a capacitor and outputs the clock stop signal based on the clock signal and a charge signal based on a charge on the capacitor, and~~

~~wherein the capacitor is selected such~~

~~that the capacitor is not discharged to a point where the charge signal transitions, when the clock signal is active, and~~

~~that the capacitor is discharged to the point where the charge signal transitions, when the clock signal is not active.~~

wherein the clock stop detector comprises:

a first switch that closes in response to a first logic level of an inverted clock signal to charge a capacitor;

a second switch that closes in response to a second logic level of the inverted clock signal to discharge the capacitor; and

a logic circuit that receives the clock signal and a charge signal based on a charge on the capacitor, and that outputs a control signal indicating when the

clock signal was not active for a period of time exceeding the predetermined period of time,

wherein the capacitor is charged to the second logic level when the inverted clock signal is at the first logic level, and

wherein the capacitor is discharged to the first logic level when the inverted clock signal is at the second logic level for a period of time exceeding the predetermined period of time.

30. (Cancelled)

31. (Original) The portable electronic device of claim 29, wherein the portable electronic device comprises one of a cellular telephone, a personal digital assistant, a music player, a game system, a digital camera, and a computer.

32. (Previously Presented) A memory comprising:

a clock stop detector configured to receive a clock signal and output a control signal in response to the clock signal;

a peripheral circuit for reading and writing data to a memory bank, wherein the peripheral circuit is configured to receive the control signal and activate and deactivate in response to the control signal; and

a data receiver and driver configured to receive the control signal and activate and deactivate in response to the control signal.

33-37. (Cancelled)

38. (Previously Presented) A memory comprising:

a clock stop detector configured to receive a clock signal and output a control signal in response to the clock signal;

a peripheral circuit for reading and writing data to a memory bank, wherein the peripheral circuit is configured to receive the control signal and activate and deactivate in response to the control signal; and

an address receiver configured to receive the control signal and activate and deactivate in response to the control signal.

39. (Previously Presented) A memory comprising:

a clock stop detector configured to receive a clock signal and output a control signal in response to the clock signal;

a peripheral circuit for reading and writing data to a memory bank, wherein the peripheral circuit is configured to receive the control signal and activate and deactivate in response to the control signal; and

a command receiver configured to receive the control signal and activate and deactivate in response to the control signal.